In the Specification

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with a power in the range of approximately 10-50 watts of DC power. An alternative p-dopant may be boron, which can be added as gaseous diborane (B_2H_6). Alternatively, the dopants can be alloyed with the silicon carbide target.

[0030] Portions of SiC layer 50 overlying the third active layer 16 may be mechanically or chemically removed to expose portions of layer 16, leaving SiC material 50 at least partially within openings 20, as illustrated in FIG. 6.

[00311 Illustrated in FIG. 7, a metal layer 70 may be deposited on the heavily doped silicon carbide ~~60~~ 50. The metal layer 70 may be aluminum or any other metal that can form an ohmic contact to p-doped silicon carbide. A metal layer 72 may be deposited on n-doped silicon carbide layer 16. The metal layer 72 on layer 16 can be nickel or any other metal that can form an ohmic contact to n-doped silicon carbide. The metal layers 70 and 72 can be deposited by any of a number of methods, including DC sputtering, RF sputtering, thermal evaporation, e-beam evaporation and chemical vapor deposition. The metal layers 70 and 72 may be patterned by photolithography and wet or dry chemical etching.

[0032] The metal layers 70 and 72 can be annealed to form an ohmic electrical connection or contact with the underlying silicon carbide. Depending upon the metal, the annealing temperature

may be in a range of approximately 600 ° C 1100°C, which is below the melting temperature of the insulating layer 30. Due to the thickness of the heavily doped silicon carbide layer 50, the reaction region 74 between the metal contact 70 and the heavily doped silicon carbide 50 that occurs when the metal is annealed should not extend through the thin layer 14. In this particular embodiment, region 74 does not physically contact layer 14.

[0033] Insulating layer 80 can be deposited on layer 16 and metal layers 70 and 72 as shown in FIG. 8. Layer 80 may be an insulator such as silicon dioxide, silicon nitride, silicon oxynitride, or the like. The insulating layer 80 may then be mechanically or chemically removed to expose surfaces of metal layers 70 and 72 as illustrated in FIG. 9. Wire leads (not shown) may be soldered, bonded, or otherwise electrically connected to the metal layer 70 and 72 contacts. For basic transistor operation, an additional wire lead can be attached to layer 12 to form a substantially completed semiconductor device.